



VIRTUAL PLATFORMS: FROM CONSUMER ELECTRONICS TO CRITICAL EMBEDDED SYSTEMS

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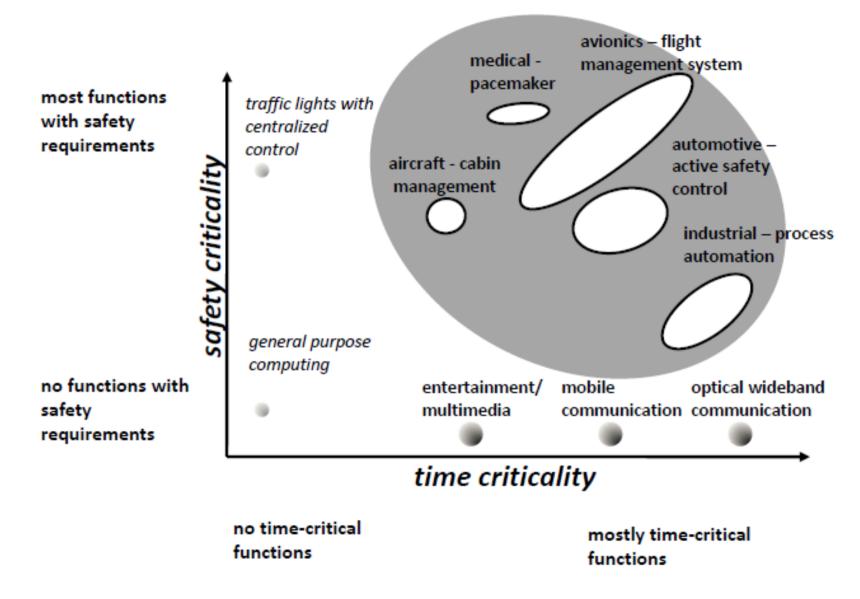
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SAFETY-CRITICAL AND TIME CRITICAL APPLICATIONS (COURTESY ROLF ERNST)







REQUIREMENTS (COURTESY ARNAUD GRASSET) **CHALLENGING NON-FUNCTIONAL**

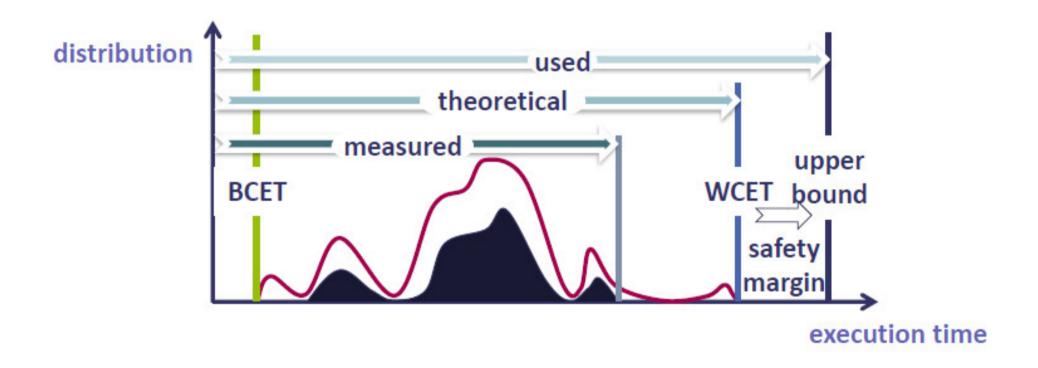






Ceatech PREDICTABILITY OF COMPLEX ARCHITECTURES

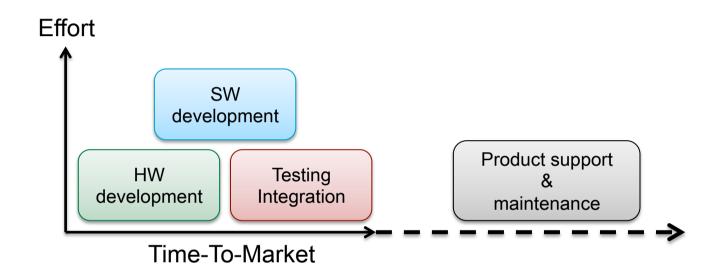






Ceatech Traditional Design and Verification Flow



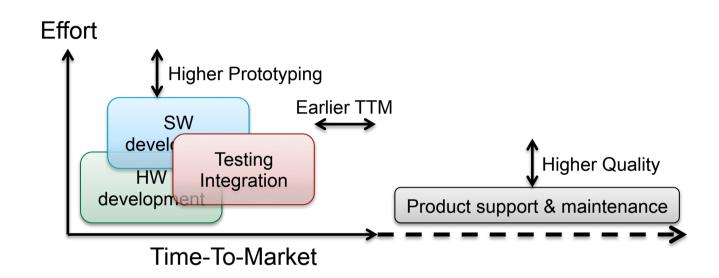


HW/SW development & testing in a pipeline



Ceatech VIRTUALIZED DESIGN AND VERIFICATION FLOW



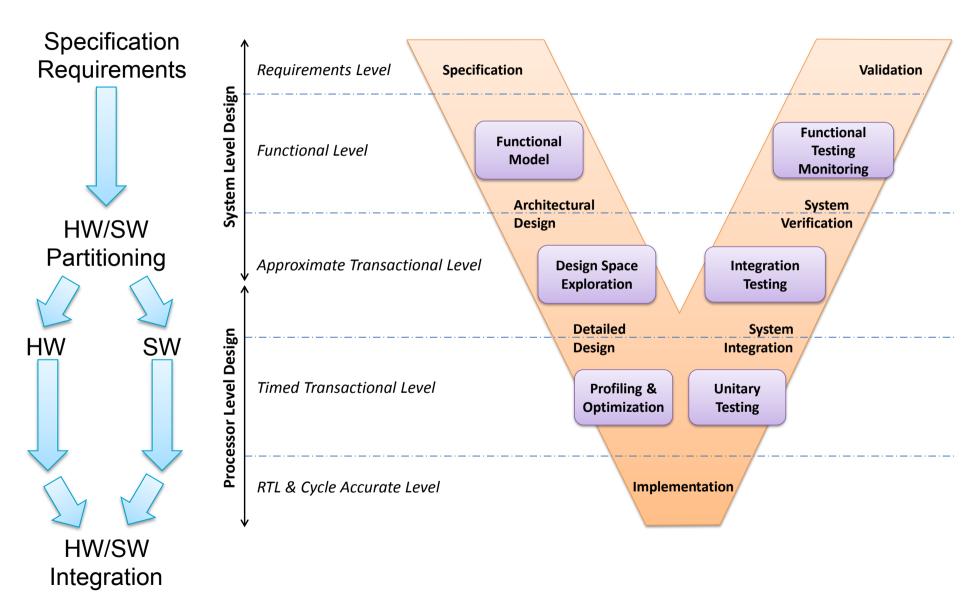


- Fusion of HW/SW development & Testing be decreased TTM
- More competitive products
- Up to 6 months faster



EMBEDDED SYSTEM DESIGN FLOW

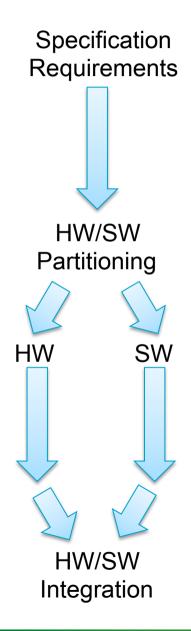






MODELING ABSTRACTION LEVELS





High Level System Model

Behavioral Model

Formal

JML, SysML

SDL

AADL

Exécutable Spécification ■UML
■AADL
■Matlab

Scilab

Modelica

Scade C/C++

SystemC ArchC

Timed Behavioral Model

Cycle Accurate Model

Approximated Timing

Annotation

Accurate Timing _C/C++ _SystemC _ArchC

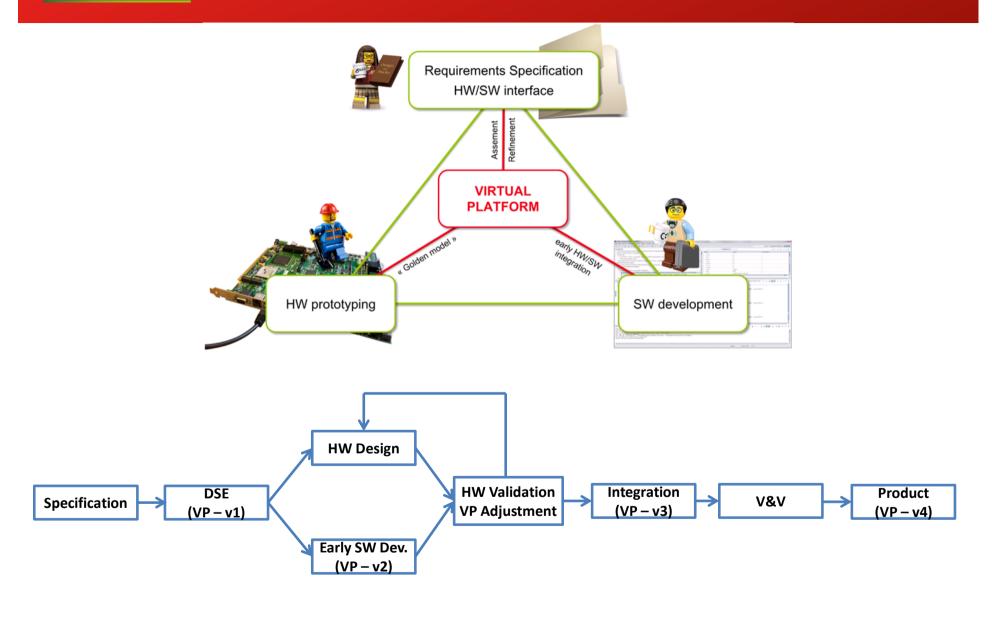
SystemC VHDL

Verilog
AMS



SIMULATION WITHIN WORKFLOW

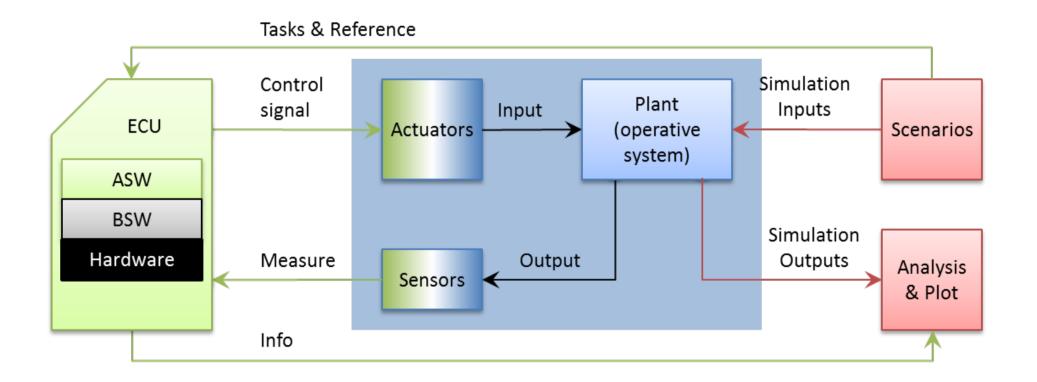






VIRTUAL TESTBED OF CONTROL LOOP





MODELING TRADEOFFS



Design/Decision criterion

- Level of detail/Precision/Representativeness
- Flexibility
- Speed
- Development cost
- Maintenance cost

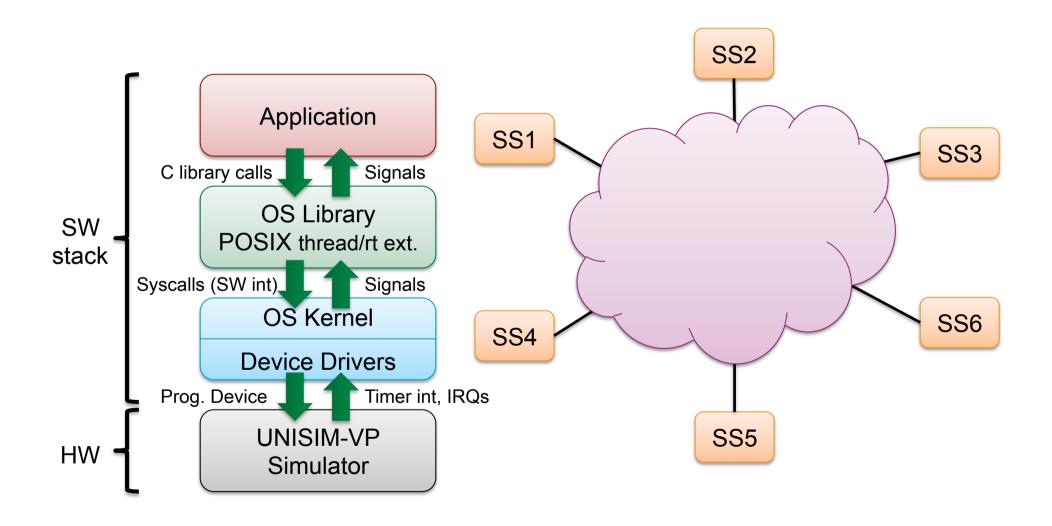
Impacts/Implications of modeling/technological choices

- Speed impacts:
 - Amount of tests
 - Quality of product because time budget for testing is limited
- **■** Low Level of Detail implies:
 - High flexibility, high speed, low cost, low maintenance cost
 - But are key characteristics still captured? Is behavior still simulated?
 - Fortunately substitutes excel sheets by fast architectural exploration
- High Level of Detail implies:
 - → igh cost & maintenance cost
 - **Low** flexibility
 - Low speed



SIMULATION SCOPE



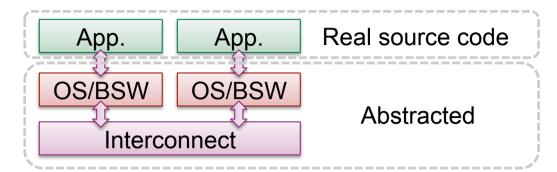




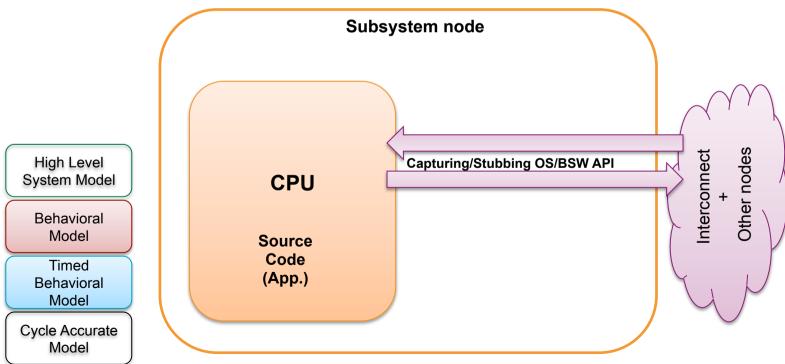
SIMULATION SCOPE – SIM2



User level: Application source code



Requires compiling target application using host compiler





SIMULATION SCOPE - SIM3

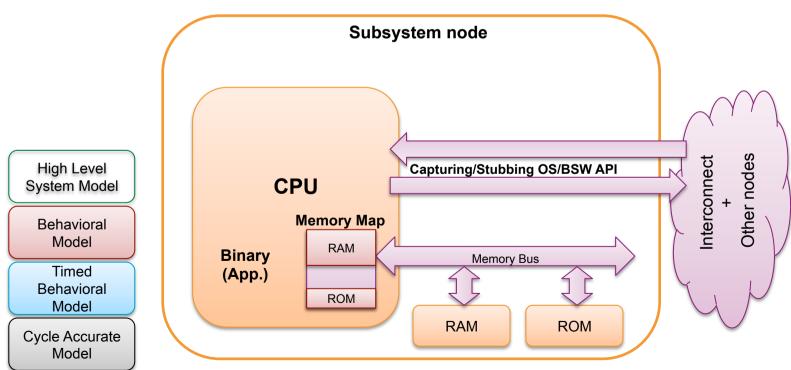


User Level: Application Binary

Requires an instruction set simulator

App. App. Real binary

OS/BSW OS/BSW
Bare Logical Model





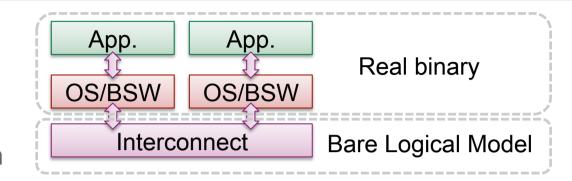
SIMULATION SCOPE - SIM4



Full system:

Application + OS binary

- Requires an instruction set simulator
- Requires simulation of peripherals

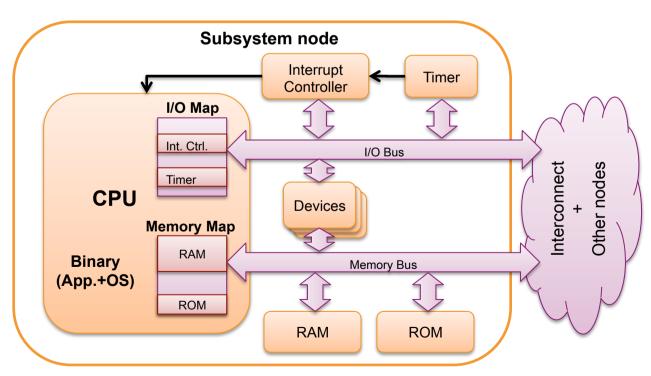


High Level
System Model

Behavioral
Model

Timed
Behavioral
Model

Cycle Accurate
Model





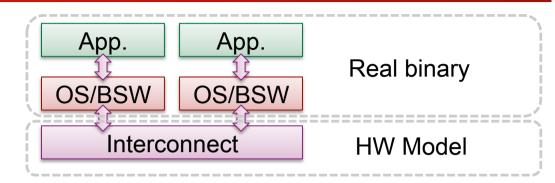
SIMULATION SCOPE – SIM5



Full system of system:

Application + OS binary

- Requires an instruction set simulator
- **■** Requires simulation of peripherals
- Requires simulation of network adapters

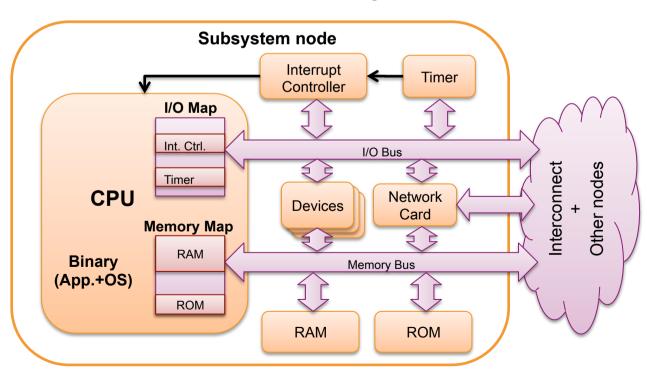


High Level
System Model

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Timed
Behavioral
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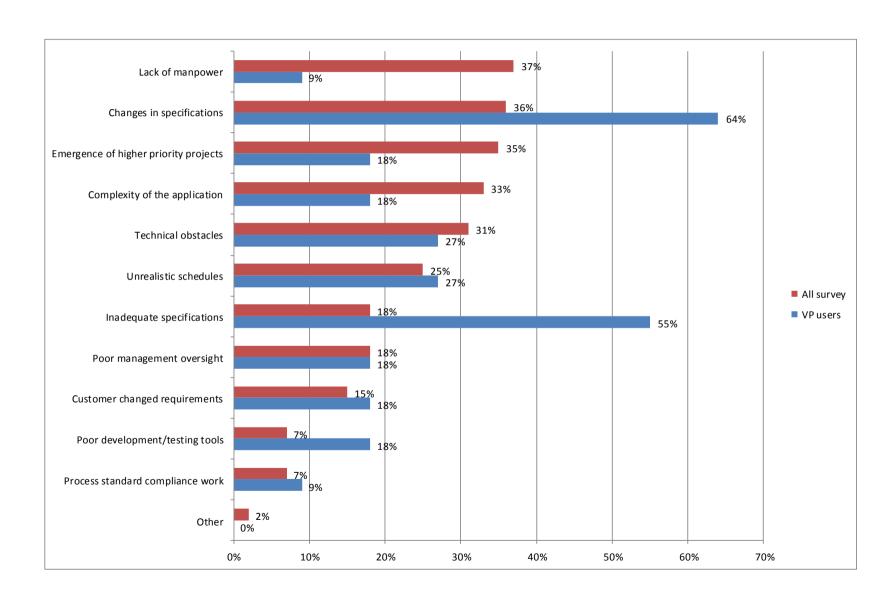
Cycle Accurate
Model





Ceatech REASONS FOR DELAYS IN PROJECT SCHEDULE



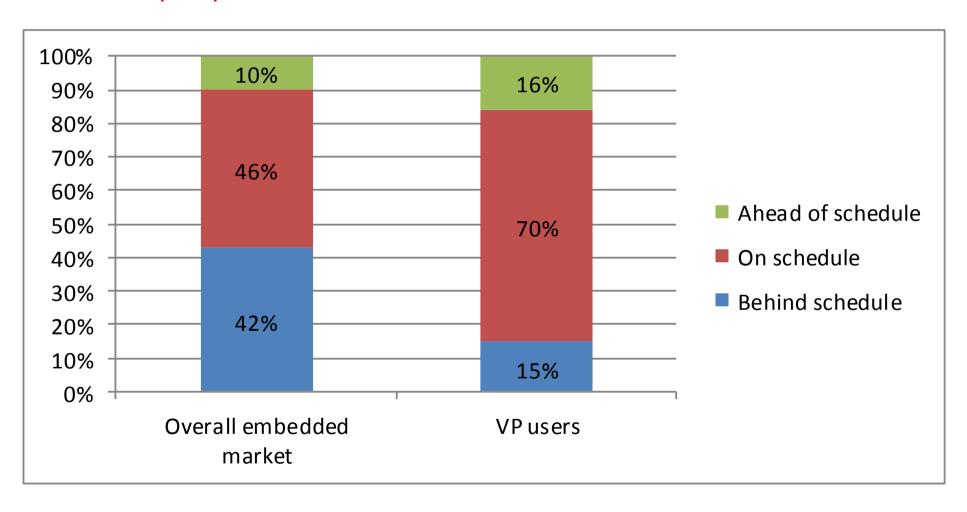




SCHEDULE ADHERENCE



COMPARISON OF OVERALL MARKET AND VIRTUAL PROTOTYPING SOLUTION (VPS) USERS





COMPETITIVE ADVANTAGES



Cheaper and Simplified deployment

- dess logistical problems (no physical constraints, no time-sharing on the board)
- Easier injection of scenarios (nominal, faults)
- Easier and extended means for system observation (traces)

Design, share and reuse

- Design space exploration
- Golden/Reference model for HW/SW architects
- Anticipated integration problems detection

Early System Validation

- Global validation of system at model level
- Multi-level co-simulation {Matlab Simulink, Statemate Stateflow, VHDL-AMS, microcontrollers UNISIM-VP}

Automation of tests

- Shorter software updates to software validation cycles
- →ess hardware manipulations: Software engineer can spend time to increase quality and validation, not manipulation

WHAT IS BLOCKING?



- **■** Current offers are not adapted to embedded systems integrators
 - ■Target the semiconductor world (hardware prototyping and verification)
 - Few instrumentation capabilities for SW verification
 - → imited interoperability (models and tools)
 - Few catalogs / suppliers
- **■** Even if the scope is limited, there are still problems
 - Development time and high cost
 - Difficulties to support in-house maintenance and upgrades of VP
 - →ow ROI when product life cycle is short
 - Early availability of VP to maximize ROI
- No open-source solution that guarantees long term support to industrial



WHAT WE SUGGEST



- Creating a virtualization ecosystem suitable for system integrators and SMEs
- Sharing of development costs
- A participatory academic/industrial consortium?
 - To benefit to all stakeholders in the value chain
 - Reduce development costs of virtual platforms
 - Increase the availability of VPs
 - Influence the market of VPs
 - Will enable more R&D activities using/around virtual platforms





QUESTIONS?