Formal Specification of Delta MINs for MPSOC in the ACL2 Logic

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Abstract

The design of modern multiprocessor systems-on-chip has performance constraints which must be satisfied by the interconnection architecture. Multistage Interconnection Networks, also denoted MINs, seem to be a promising alternative for solving the problems of on-chip communications. This paper presents a formal specification of the Delta multistage interconnection networks for MPSoCs in the ACL2 logic. This work is based on a generic model for networks on chip (GeNoC).

1. Introduction

MPSOC platforms that will be used in future generations must satisfy many critical requirements: they have to be energy efficient, cheap, reliable, and must offer sufficient computing power.

Networks on Chip (NoCs) have been proposed by academia and industry as a solution for the on-chip communication challenges in the future MPSoCs [1]. The Multistage Interconnection Networks (MINs) can be a promising alternative for NoCs [2]. Although these networks have been extensively studied in the off-chip context; they have been frequently used in classical multiprocessor systems like IBMSP [3], and in ATM switches [4], their study to implement NoCs is new.

A key step in the design of MPSoCs is the verification of the whole system, and especially of the selected communication architecture. When applied by simulation [5], the verification is partial. The new trend is then to adopt formal verification.

A Formal specification of Delta MINs for MPSOC in the ACL2 logic is investigated in this paper. In section 2, MIN architecture is presented. Next, we briefly introduce the generic model GeNoC. Finally, we detail the formal model developed to specify the Delta MINs, and discuss future works.

2. Basic MIN

The multistage interconnection networks can provide a maximum bandwidth to components (IP, DSP, processors…), a minimum delay access to memory modules, and can be dynamically reconfigurable [6].

An example of Delta networks (a subclass of MINs) illustrated in figure 1 connects 8 processors to 8 memories by means of 3 stages of 4 switches each. Processors and memories are represented by 3-bit number $(d_2\ d_1\ d_0)_2$. The interconnection stages denoted C_i $(0 \leq i \leq 3)$ are generated by applying permutation functions. A path between a source and a target is obtained by operating a switch at stage S_i through the upper output if the i^{th} bit (d_i) of the destination address is equal to 0, otherwise through the lower output.

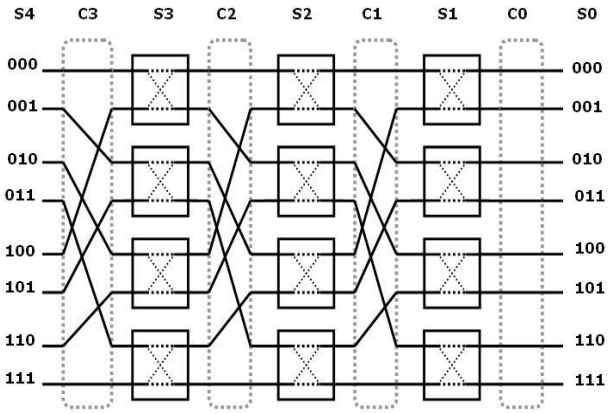

Figure 1. A Delta network (8,2)

2. GeNoC overview

GeNoC (Generic Networks on Chip) is a generic and formal model describing communications in NoCs. Several NoCs like the Octagon and the Mesh 2D were specified and validated by applying the GeNoC approach [7]. The GeNoC model has been also extended to verify communications in the Hermes NoC [8].

As defined in GeNoC, the routing function supposes the existence of connections between two successive nodes of a computed route. It was possible to validate the Octagon and the XY routing algorithms through GeNoC because these algorithms give explicitly the next node of a route. The routing algorithm in Delta networks is different: by giving only the port through which the message must be switched, it doesn't give any indication about the position of the next switch. As a result, and given the importance of the topological aspect of Delta networks, we notice that applying the actual GeNoC model to validate the Delta routing algorithm is impossible without taking into account the connection aspect of the network. So, the connection component has to be involved in the formal model.

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3. Formal specification of Delta-MINs

In this section, we give a formal specification of Delta networks. First, we deal with topology which is composed of nodes and connections.

3.1. The topology component

-*The set of nodes*: a pair of coordinates (x y) is used to represent a node in a Delta MIN. The coordinate x is decimal. It represents the stage of nodes to which belongs the node. The Y coordinate is binary and it describes the position of the node within the same stage. The function *gen-nodes-dmin* generates all nodes of the network. It takes as parameters *N*, the size of the network, and *r* (r=2), the degree of switches. The validity of these parameters is recognized by the predicate *ValidParamsp-dmin*. We define also another predicate called *dmin-nodesetp* for the whole nodes validity. The nodes set generation is constrained by the theorem 1, which is an instance of the main GeNoC constraint on the set of nodes.

Theorem 1. Nodes set generation

```
(defthm gen-nodes-dmin-correct
 (implies (ValideParams-dmin pms)
          (dmin-nodesetp (gen-nodes-dmin pms)))
```

- *Connections*: we represent a connection *cnx* in a Delta MIN by a list *((x px) (y py))*, where *x* is the origin of *cnx*, *px* is the first switch port involved in *cnx*, *y* is the second extremity and *py* is the port of *y*. For example, the connection ((((3) (01)) O0) (((2) (10)) I0)) denotes that the port "O0"of the switch ((3) (01)) is connected to the port "I0" of ((2) (10)). All connections are obtained by operating permutation functions: a list of three functions to apply respectively for the first connection stage, the middle stages, and on the last stage.

3.2. The routing component

The routing function *routing-dmin* takes as arguments the list of messages to be routed through the Delta MIN, and the parameters for generating the whole topology. For each message, *routing-dmin* calls the function *compute-rtes-dmin* (definition 1) to compute the routes between the origin (*from*) and the destination (*dest*). After testing the i^{th} bit of the destination address *(dest [i])* which gives the port whereby the message must be switched at the crossbar of the stage S_i, the function *rech_top* is used to give the next switch connected to this port.

Definition 1. Function compute-rte

```
compute-rtes-dmin (from dest top)
if (from = dest)    /* destination reached */
then take the local port of the destination
else
 if (dest [i] = 0) /* ith bit equals 0 */
 then take the upper output of the switch at Si
      from = rech_top (from top 0)
 else /* ith bit equals 1 */
      take the lower output of the switch at Si
      from = rech_top (from top 1)
```

We simulate the execution of the definitions in the ACL2 theorem proving environment. We present below a simulation of the function *routing-dmin* showing the progression of the list of messages illustrated in table 1 through a Delta network 8 x 8, using 2 x 2 crossbars.

Table 1. The list of messages

id	*origin*	*content*	*destination*
1	((4) (001))	frm1	((0) (100))
2	((4) (101))	frm2	((0) (001))

The computed route of the first message is shown below (table 2). We can notice that the routing makes use of connections like ((((3) (01)) O1) (((2) (11)) I0)), to compute a route.

Table 2. The computed route of message 1

stage	1
C3	((((4) (001)) O) (((3) (01)) I0))
C2	((((3) (01)) O1) (((2) (11)) I0))
C1	((((2) (11)) O0) (((1) (10)) I1))
C0	((((1) (10)) O0) (((0) (100)) I))

4. Conclusion and future works

In this paper, we have proposed a formal specification of the Delta multistage interconnection networks in the ACL2 logic. The formal specification is developed by applying a generic model for networks on chip model (GeNoC). We are aware that the application of this generic model to our case study requires its extension. We plan to achieve this extension by developing a generic topology and the consequent extended routing component.

5. References

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