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SCAC

Synchronous Communication Asynchronous Computation:

An Execution Model for Massively Parallel Architecture

Existing Massively Parallel Processing Architectures

SIMD
- Synchronous execution mode
- Hardware cost : cheap ✓ (1 CU, 1 copy of instructions)
- Data parallelism ✗ (limited applicability)
- Execution time: ✗ $T(SIMD)=Max\{t_1\}+Max\{t_2\}+\dots+Max\{t_n\}$

MIMD
- Asynchronous execution mode
- Hardware cost : Expensive ✗ (Many CUs, Program stored at each processor)
- Functional parallelism ✓ (general purpose)
- Execution time: ✓ $T(MIMD)=Max\{t_1+t_2+\dots+t_n\}$

Solution

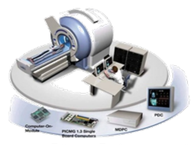
Heterogeneous mixed-mode SIMD/SPMD Execution model (SCAC)
"Synchronous Communication & Asynchronous Computation"

High Performance and High Flexibility

Requirements of compute-intensive media applications


video compression


image processing


medical imaging

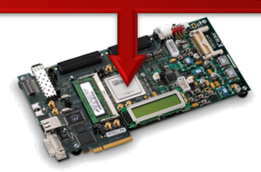

software defined radio

High Performance
Time execution
Bandwidth

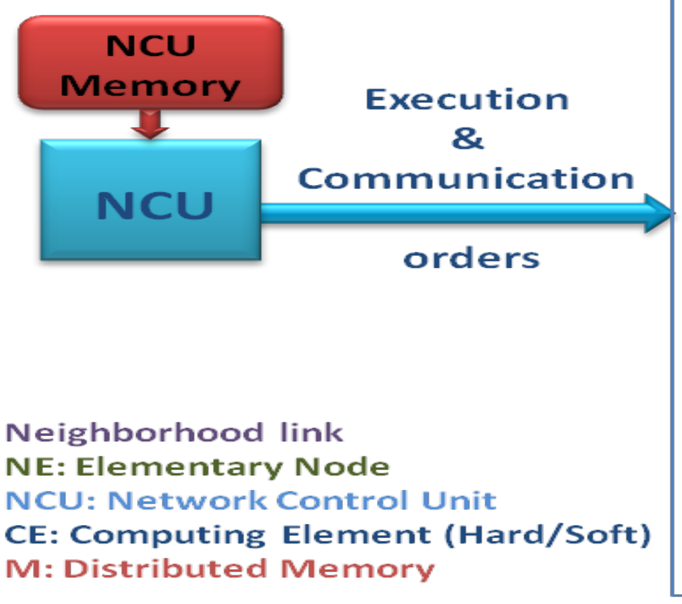
High Flexibility
Application variety

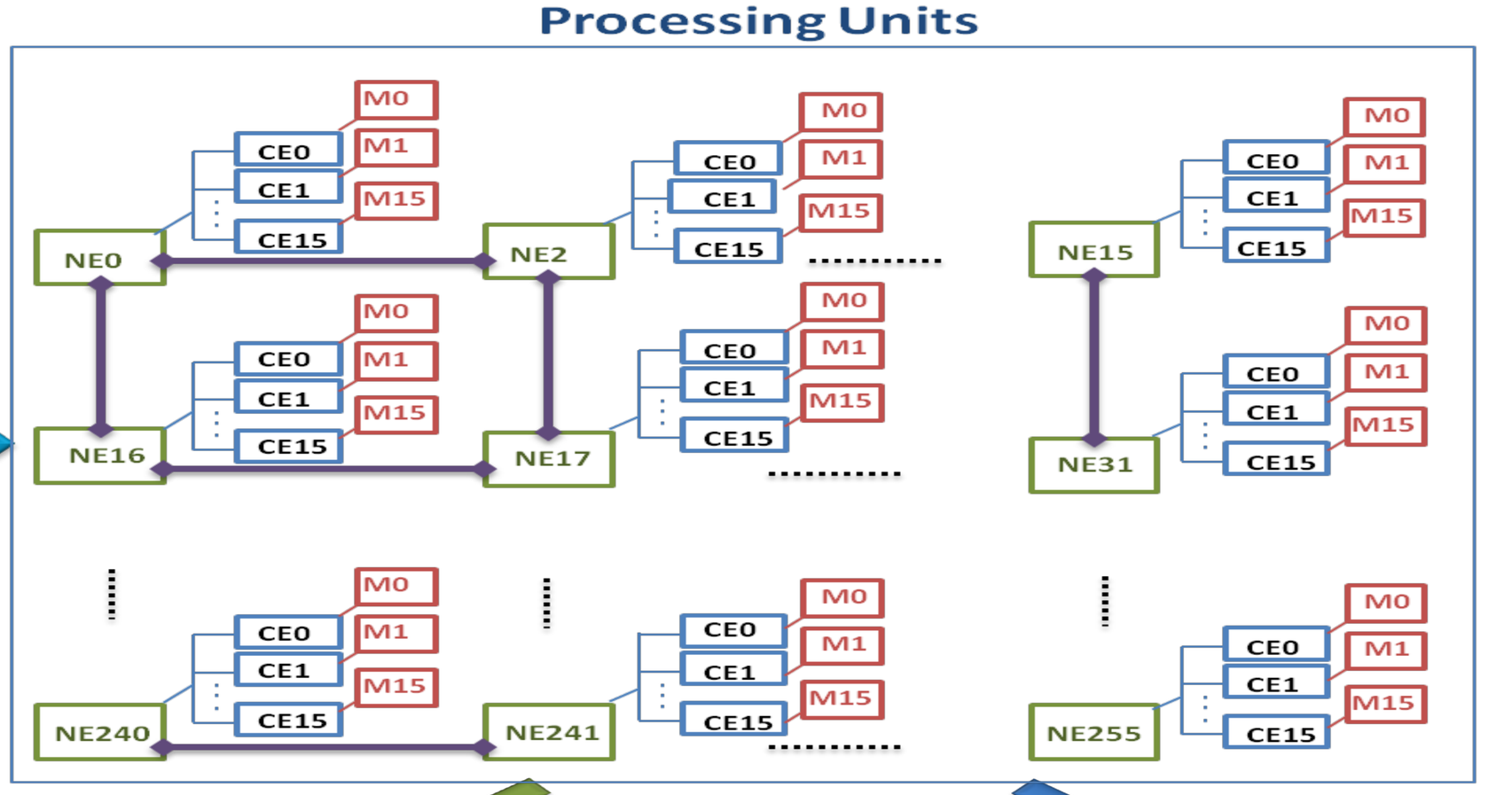
Power Efficiency
Low price (small die size)
Easy cooling (~3W)

Same silicon circuit for many applications

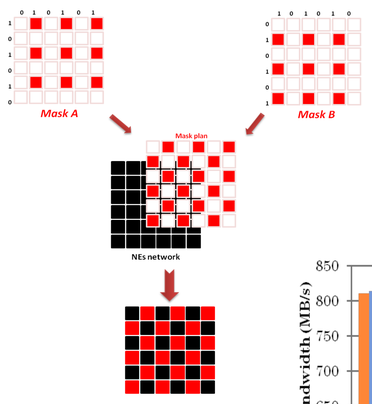


SCAC Execution Model

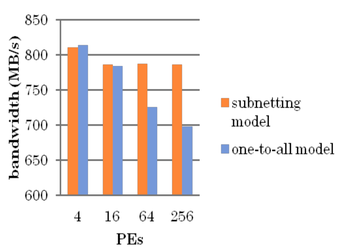


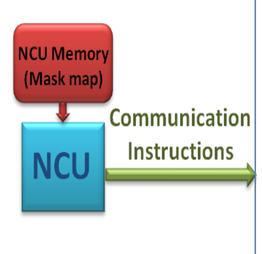


Communication Master - Slave: Broadcast with Mask

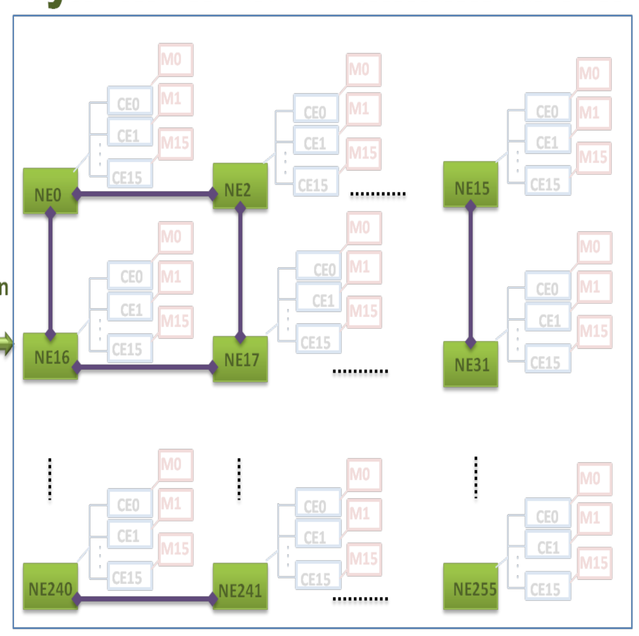


	Broadcast with mask	Broadcast one-to-all
Fmax(Mhz)	205.999	182.846
Bandwidth(MB/s)	786	697
Power supply (w)	3.214	4.447
Latency (cycles)	3	16

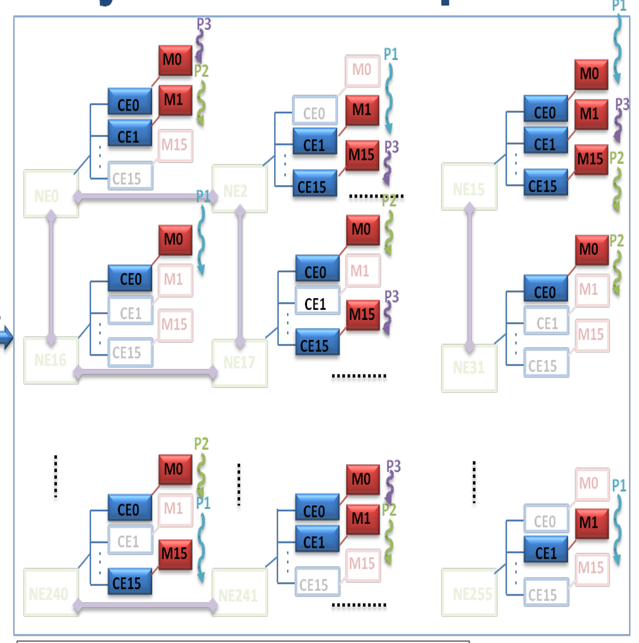




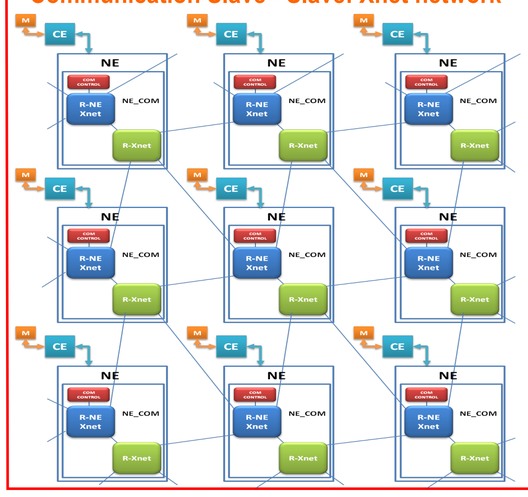
Synchronous Communication

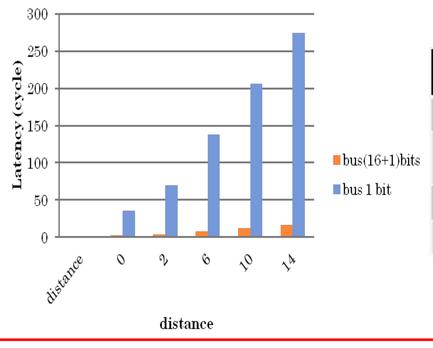


Asynchronous Computation

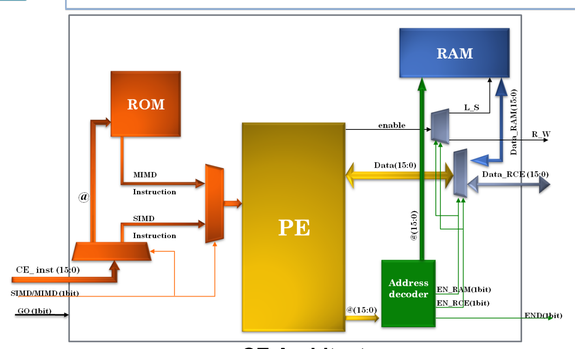


Communication Slave - Slave: Xnet network





	Bus (16+1) bits	Bus 1 bit	FPGA resources
Fmax(Mhz)	263.912	183.839	-
Latency (cycles)	Dist+2	(16+1)(Dist+2)+2 = 17 dist + 36	-
register	35328	13824	948480
LUT	100820	44512	474240



CE Architecture